59. (**Amended**) A method of simulating Euclidean wiring in an integrated circuit layout, said method comprising:

determining a preferred wiring angle for a metal layer of said integrated circuit layout;

determining a ratio of first interconnect line length along a first direction to a second interconnect line length along a second direction that is approximately 45 degrees from said first direction to create a simulated interconnect line along said preferred wiring angle; and

routing said metal layer using said preferred wiring angle by creating interconnect wires made up of wire segments of said first interconnect line length along said first direction and wire segments of said second interconnect line length along said second direction.

60. (**Amended**) The method of claim 59 wherein said first direction is horizontal and said second direction is substantially 45 degrees from said horizontal.

61. (**Amended**) The method of according to claim 59 further comprising:

routing a first interconnect line along said preferred wiring angle by connecting alternating pairs of said first interconnect line length along said first direction and said second interconnect line length along said second direction.

62. (**Amended**) A method of simulating Euclidean wiring, said method comprising:

determining a preferred wiring angle for a metal layer;

A2

determining a ratio of a first interconnect line length along a first direction to a second interconnect line length along a second direction that is substantially orthogonal to said first direction to create a simulated interconnect line along said preferred wiring angle; and

routing said metal layer using said preferred wiring angle.

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64. (**Amended**) The method of according to claim 62 further comprising:

routing a first interconnect line along said preferred wiring angle by connecting alternating pairs of an interconnect line length along said first direction and an a substantially orthogonal interconnect line length along said second direction.

A3

65. (**Amended**) An integrated circuit layout, said integrated circuit layout comprising:

a plurality of circuit modules;

a first interconnect line layer, said first interconnect line layer having a preferred horizontal direction of interconnect lines;

a second interconnect line layer, said second interconnect line layer with having a preferred vertical direction of interconnect lines; and

a third interconnect line layer, said third interconnect line layer having a first arbitrary diagonal preferred direction;

wherein interconnect lines on said third interconnect line layer comprise a plurality of alternating interconnect line subsegments wherein a first subsegment is horizontal and a second subsegment is approximately 45 degrees diagonal to said horizontal.

A3

66. (**Amended**) The integrated circuit layout as claimed in claim 65, said integrated circuit layout further comprising:

a fourth interconnect line layer, said fourth interconnect line layer having a second diagonal preferred direction, said second diagonal preferred direction substantially orthogonal to said first diagonal preferred direction wherein interconnect lines on said fourth interconnect line layer comprise a plurality of alternating interconnect line subsegments.

68. (**Amended**) The integrated circuit layout as claimed in claim 66, said integrated circuit layout further comprising:

A4

a fifth interconnect line layer, said fifth interconnect line layer having a second diagonal preferred direction, said second diagonal preferred direction substantially orthogonal to said first diagonal preferred direction wherein interconnect lines on said fifth interconnect line layer comprise a plurality of alternating interconnect line subsegments.

69. (**Amended**) A method of laying out an integrated circuit, said method comprising:

placing a plurality of circuit modules;

routing a first interconnect line layer, said first interconnect line layer having a preferred horizontal direction of interconnect lines;

routing a second interconnect line layer, said second interconnect line layer with having a preferred vertical direction of interconnect lines; and

routing a third interconnect line layer, said third interconnect line layer having a first preferred diagonal direction;

wherein interconnect lines on said third interconnect line layer comprise a plurality of alternating interconnect line subsegments wherein a first subsegment is horizontal and a second subsegment is approximately 45 degrees diagonal to said horizontal.

70. (**Amended**) The method of laying out said integrated circuit layout as claimed in claim 69, said method further comprising:

routing a fourth interconnect line layer, said fourth interconnect line layer having a second diagonal preferred direction, said second diagonal preferred direction substantially orthogonal to said first diagonal preferred direction wherein interconnect lines on said fourth interconnect line layer comprise a plurality of alternating interconnect line subsegments.

Please add the following claims:

72. (**Added**) A method of laying out an integrated circuit, said method comprising:

placing a plurality of circuit modules;

routing a first interconnect line layer, said first interconnect line layer having a preferred horizontal direction of interconnect lines;

routing a second interconnect line layer, said second interconnect line layer with having a preferred vertical direction of interconnect lines; and

routing a third interconnect line layer, said third interconnect line layer having a first preferred diagonal direction;

wherein interconnect lines on said third interconnect line layer comprise a plurality of alternating interconnect line subsegments wherein a first subsegment is horizontal and a second subsegment is substantially orthogonal to said horizontal.

73. (**Added**) The method of laying out said integrated circuit layout as claimed in claim 72, said method further comprising:

routing a fourth interconnect line layer, said fourth interconnect line layer having a second diagonal preferred direction, said second diagonal preferred direction substantially orthogonal to said first diagonal preferred direction wherein interconnect lines on said fourth interconnect line layer comprise a plurality of alternating interconnect line subsegments.

74. (**Added**) The method of laying out said integrated circuit layout as claimed in claim 72, said method wherein said first diagonal preferred direction is approximately forty-five degrees relative to said preferred horizontal direction and said second diagonal preferred direction is approximately negative forty-five degrees relative to said preferred horizontal direction.

AS

The Amended Claims

The following pages provide the amended claims with the amendments marked with deleted material in [brackets] and new material underlined.

59. (**Amended**) A method of simulating Euclidean wiring in an integrated circuit layout, said method comprising:

determining a preferred wiring angle for a metal layer of said integrated circuit layout;

determining a ratio of [an] first interconnect line length along a first direction to a second [diagonal] interconnect line length along a second direction that is approximately 45 degrees from said first direction to create a simulated interconnect line along said preferred wiring angle; and

routing said metal layer using said preferred wiring angle by creating interconnect wires made up of wire segments of said first interconnect line length along said first direction and wire segments of said second interconnect line length along said second direction.

60. (**Amended**) The method of claim 59 wherein said first direction is horizontal and said second direction is substantially 45 degrees from said horizontal.

61. (**Amended**) The method of according to claim 59 further comprising:

routing a first interconnect line along said preferred wiring angle by connecting alternating pairs of said first [an] interconnect line length along said first direction and [a] said second [diagonal] interconnect line length along said second direction.

62. (**Amended**) A method of simulating Euclidean wiring, said method comprising:

determining a preferred wiring angle for a metal layer;

determining a ratio of a first interconnect line length along a first direction to a second interconnect line length along a second direction that is [approximately 90 degrees from] substantially orthogonal to said first direction to create a simulated interconnect line along said preferred wiring angle; and

routing said metal layer using said preferred wiring angle.

64. (**Amended**) The method of according to claim 62 further comprising:

routing a first interconnect line along said preferred wiring angle by connecting alternating pairs of an interconnect line length along said first direction and an a substantially orthogonal [orthognal] interconnect line length along said second direction.

65. (**Amended**) An integrated circuit layout, said integrated circuit layout comprising:

a plurality of circuit modules;

a first interconnect line layer, said first interconnect line layer having a preferred horizontal direction of interconnect lines;

a second interconnect line layer, said second interconnect line layer with having a preferred vertical direction of interconnect lines; and

a third interconnect line layer, said third interconnect line layer having a first arbitrary diagonal preferred direction;

wherein interconnect lines on said third interconnect line layer comprise a plurality of alternating interconnect line subsegments wherein a first subsegment is horizontal and a second subsegment is approximately 45 degrees diagonal to said horizontal [first subsegment].

66. (**Amended**) The integrated circuit layout as claimed in claim 65, said integrated circuit layout further comprising:

a fourth interconnect line layer, said fourth interconnect line layer having a second diagonal preferred direction, said second diagonal preferred direction substantially orthogonal to said first diagonal preferred direction wherein interconnect lines on said fourth interconnect line layer comprise a plurality of alternating interconnect line subsegments.

68. (**Amended**) The integrated circuit layout as claimed in claim 66, said integrated circuit layout further comprising:

a fifth interconnect line layer, said fifth interconnect line layer having a second diagonal preferred direction, said second diagonal preferred direction substantially orthogonal to said first diagonal preferred direction wherein interconnect lines on said fifth interconnect line layer comprise a plurality of alternating interconnect line subsegments.

69. (**Amended**) A method of laying out an integrated circuit, said method comprising:

placing a plurality of circuit modules;

routing a first interconnect line layer, said first interconnect line layer having a preferred horizontal direction of interconnect lines;

routing a second interconnect line layer, said second interconnect line layer with having a preferred vertical direction of interconnect lines; and

routing a third interconnect line layer, said third interconnect line layer having a first preferred diagonal direction;

wherein interconnect lines on said third interconnect line layer comprise a plurality of alternating interconnect line subsegments wherein a first subsegment is horizontal and a second subsegment is approximately 45 degrees diagonal to said horizontal [first subsegment].

70. (**Amended**) The method of laying out said integrated circuit layout as claimed in claim 69, said method further comprising:

routing a fourth interconnect line layer, said fourth interconnect line layer having a second diagonal preferred direction, said second diagonal preferred direction substantially orthogonal to said first diagonal preferred direction wherein interconnect lines on said fourth interconnect line layer comprise a plurality of alternating interconnect line subsegments.